In the Claims:

Claim 10 has been amended as follows:

10. (AMENDED) A method of detecting a threshold voltage implantation reticle option layer in an integrated circuit device comprising:

measuring the current through a first MOS transistor in an integrated circuit device by forcing a test voltage on the drain and the gate wherein said gate and said drain of said first MOS transistor are connected together, wherein the source of said first MOS transistor is connected to a reference voltage, and wherein said first MOS transistor has a first threshold voltage implantation but not a threshold voltage implantation reticle option layer;

measuring the current through a second MOS transistor in said integrated circuit device by forcing same said test voltage on the drain and the gate wherein said gate and said drain of said second MOS transistor are connected together, wherein the source of said second MOS transistor is connected to a reference voltage, and wherein said second MOS transistor has both said first threshold voltage

implantation and said threshold voltage implantation reticle option layer; and

comparing said current through said first MOS transistor and said current through said second MOS transistor to detect the presence of said threshold voltage implantation reticle option layer in said integrated circuit device.

Claim 15 has been amended as follows:

15. (AMENDED) A method of detecting a threshold voltage implantation reticle option layer in an integrated circuit device comprising:

selecting a first NMOS transistor in an integrated circuit device in a first test mode to couple the voltage at the drain and the gate of said first NMOS transistor to an output pin of said integrated circuit device wherein said gate and said drain of said first NMOS transistor are connected together, wherein the source of said first NMOS transistor is connected to ground, and wherein said first NMOS transistor has a first threshold voltage implantation but not a threshold voltage implantation reticle option layer;

measuring said voltage at said output pin in said first test mode when an internal test voltage is connected to said drain and said gate of said first NMOS transistor through a first internal standard resistance;

selecting a second NMOS transistor in said integrated circuit device in a second test mode to couple the voltage at the drain and the gate of said second NMOS transistor to said output pin of said integrated circuit device wherein said gate and said drain of said second NMOS transistor are connected together, wherein the source of said NMOS transistor is connected to ground, and wherein said second NMOS transistor has both said first threshold voltage implantation and said threshold voltage implantation reticle option layer;

measuring said voltage at said output pin in said second test mode when said internal test voltage is connected to said drain and said gate of said second NMOS transistor through a second internal standard resistance; and

comparing said voltage at said output pin in said first test mode with said voltage at said output pin in said second test mode to detect the presence of said

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threshold voltage implantation reticle option layer in said integrated circuit device.

Claim 20 has been amended as follows:

20. (AMENDED) A method of detecting a threshold voltage implantation reticle option layer in an integrated circuit device comprising:

selecting a first PMOS transistor in an integrated circuit device in a first test mode to couple the voltage at the drain and the gate of said first PMOS transistor to

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an output pin of said integrated circuit device wherein said gate and said drain of said first PMOS transistor are connected together, wherein the source of said first PMOS transistor is connected to an internal standard voltage, and wherein said first PMOS transistor has the standard threshold voltage implantation but not the threshold voltage implantation reticle option layer;

measuring said voltage at said output pin in said first test mode when said drain and said gate of said first PMOS transistor are connected to ground through a first internal standard resistance;

selecting a second PMOS transistor in said integrated

circuit device in a second test mode to couple the voltage at the drain and the gate of said second PMOS transistor to said output pin of said integrated circuit device wherein said gate and said drain of said second PMOS transistor are connected together, wherein the source of said second PMOS transistor is connected to said internal standard voltage, and wherein said second PMOS transistor has both said standard threshold voltage implantation and said threshold voltage implantation reticle option layer;

measuring said voltage at said output pin in said second test mode when said drain and said gate of said second PMOS transistor are connected to said ground through a second internal standard resistance; and

comparing said voltage at said output pin in said first test mode with said voltage at said output pin in said second test mode to detect the presence of said threshold voltage implantation reticle option layer in said integrated circuit device.